

What is claimed is:

- 1 1. A module comprising:
2 a substrate;
3 a first microelectronic die mounted on said substrate, said first microelectronic
4 die including a first receiver front end to process a signal received by a first antenna;
5 a second microelectronic die mounted on said substrate, said second
6 microelectronic die including a second receiver front end to process a signal received by
7 a second antenna;
8 a third microelectronic die mounted on said substrate, said third microelectronic
9 die including analog baseband circuitry to process baseband output signals of said first
10 and second receiver front ends;
11 a first interconnect coupled between an output of said first microelectronic die
12 and a first input of said third microelectronic die; and
13 a second interconnect coupled between an output of said second microelectronic
14 die and a second input of said third microelectronic die.

- 1 2. The module of claim 1, wherein:
2 at least one of said first interconnect and said second interconnect includes a
3 differential transmission line.

- 1 3. The module of claim 1, wherein:
2 at least one of said first interconnect and said second interconnect includes a
3 metallization portion formed on a surface of said substrate.

- 1 4. The module of claim 1, wherein:
2 at least one of said first interconnect and said second interconnect includes a
3 microstrip transmission line formed on said substrate.

1 5. The module of claim 1, wherein:
2 said substrate includes a ground plane that forms a part of said first and second
3 interconnects.

1 6. The module of claim 1, wherein:
2 said substrate includes a dielectric board material.

1 7. The module of claim 1, wherein:
2 said substrate includes alumina.

1 8. The module of claim 1, wherein:
2 said substrate includes a semiconductor material.

1 9. The module of claim 1, comprising:
2 at least one first terminal for connection to a first external antenna, said at least
3 one first terminal being coupled to said first microelectronic die; and
4 at least one second terminal for connection to a second external antenna, said at
5 least one second terminal being coupled to said second microelectronic die.

1 10. The module of claim 1, comprising:
2 a third interconnect coupled between said first microelectronic die and said
3 second microelectronic die.

1 11. The module of claim 10, wherein:
2 said first receiver front end includes a first low noise amplifier (LNA) to
3 amplify a signal from a first antenna and a first mixer to frequency convert an output
4 signal of said first LNA; and
5 said second receiver front end includes a second LNA to amplify a signal from a
6 second antenna and a second mixer to frequency convert an output signal of said second
7 LNA;

8 wherein said second microelectronic chip further includes a voltage controlled
9 oscillator to generate local oscillator signals for said first and second mixers, said third
10 interconnect to carry a corresponding local oscillator signal to said first microelectronic
11 die for use by said first mixer.

1 12. The module of claim 1, comprising:

2 a fourth microelectronic die mounted on said substrate, said fourth
3 microelectronic die including a third receiver front end to process a signal received by a
4 third antenna; and

5 a fourth interconnect coupled between an output of said fourth microelectronic
6 die and a third input of said third microelectronic die.

1 13. A multi-antenna receiver system, comprising:

2 a first low noise amplifier (LNA) having a differential input to receive a signal
3 from a first antenna;

4 a second LNA having a single-ended input to receive a signal from a second
5 antenna;

6 a first mixer to perform a frequency conversion on an amplified output signal of
7 said first LNA;

8 a second mixer to perform a frequency conversion on an amplified output signal
9 of said second LNA; and

10 a voltage controlled oscillator (VCO) to provide a local oscillator signal to said
11 first and second mixers.

1 14. The receiver system of claim 13, wherein:

2 said first and second LNAs, said first and second mixers, and said VCO are
3 implemented on a common semiconductor chip.

1 15. The receiver system of claim 13, further comprising:
2 a first filter to filter a frequency converted output signal of said first mixer, said
3 first filter having an output for connection to a first analog to digital (A/D) converter;
4 and
5 a second filter to filter a frequency converted output signal of said second mixer,
6 said second filter having an output for connection to a second A/D converter.

1 16. The receiver system of claim 15, wherein:
2 said first and second LNAs, said first and second mixers, said VCO, and said
3 first and second filters are implemented on a common semiconductor chip.

1 17. The receiver system of claim 13, further comprising:
2 a prescaler to count down an output frequency of said VCO for use in a
3 feedback loop of a corresponding phased locked loop (PLL), wherein said first and
4 second LNAs, said first and second mixers, said VCO, and said prescaler are
5 implemented on a common semiconductor chip.

1 18. The receiver system of claim 13, further comprising:
2 a third LNA having a single-ended input to receive a signal from a third
3 antenna; and
4 a third mixer to perform a frequency conversion on an amplified output signal of
5 said third LNA.

1 19. A system comprising:
2 a first patch antenna;
3 a second patch antenna;
4 a substrate;
5 a first microelectronic die mounted on said substrate, said first microelectronic
6 die including a first receiver front end to process a signal received by said first patch
7 antenna;

8 a second microelectronic die mounted on said substrate, said second
9 microelectronic die including a second receiver front end to process a signal received by
10 said second patch antenna;

11 a third microelectronic die mounted on said substrate, said third microelectronic
12 die including analog baseband circuitry to process baseband output signals of said first
13 and second receiver front ends;

14 a first interconnect coupled between an output of said first microelectronic die
15 and a first input of said third microelectronic die; and

16 a second interconnect coupled between an output of said second microelectronic
17 die and a second input of said third microelectronic die.

1 20. The system of claim 19, wherein:
2 said system includes a handheld communicator.

1 21. The system of claim 19, wherein:
2 said first and second interconnects include differential transmission lines.

1 22. The system of claim 19, wherein:
2 said first and second interconnects include metallization portions formed on a
3 surface of said substrate.

1 23. The system of claim 19, wherein:
2 said first and second interconnects are microstrip transmission lines formed on
3 said substrate.

1 24. The system of claim 19, wherein:
2 said substrate includes a dielectric board material.

1 25. The system of claim 19, wherein:
2 said substrate includes a semiconductor material.

1 26. The system of claim 19, wherein:
2 said substrate, said first, second, and third microelectronic dice, and said first
3 and second interconnects are part of a single receiver module.

1 27. A method comprising:
2 amplifying a first signal received by a first antenna using a differential low noise
3 amplifier (LNA) to generate an amplified first signal;
4 amplifying a second signal received by a second antenna using a single ended
5 LNA to generate an amplified second signal; and
6 processing said amplified first signal and said amplified second signal to
7 generate a single receiver output signal.

1 28. The method of claim 27, wherein:
2 processing includes frequency converting said amplified first signal and said
3 amplified second signal.

1 29. The method of claim 28, wherein:
2 processing includes filtering said amplified first signal and said amplified
3 second signal after frequency converting.

1 30. The method of claim 29, wherein:
2 processing includes converting said amplified first signal and said amplified
3 second signal to a digital format after filtering to generate a digitized first signal and a
4 digitized second signal.

1 31. The method of claim 30, wherein:
2 processing includes digitally processing said digitized first signal and said
3 digitized second signal together to generate said single receiver output signal.